Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. OE**
2. **Q0**
3. **D0**
4. **D1**
5. **Q1**
6. **Q2**
7. **D2**
8. **D3**
9. **Q3**
10. **GND**
11. **N. LE**
12. **Q4**
13. **D4**
14. **D5**
15. **Q5**
16. **Q6**
17. **D6**
18. **D7**
19. **Q7**
20. **VCC**

**.069”**

**.076”**

**3 2 1 20 19 18**

**8 9 10 11 12 13**

**17**

**16**

**15**

**14**

**4**

**5**

**6**

**7**

**MASK**

**REF**

**HCT373T**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vcc**

**Mask Ref: HCT373T**

**APPROVED BY: DK DIE SIZE .069” X .077” DATE: 8/26/21**

**MFG: TEXAS INSTRU/HARRIS THICKNESS .011” P/N: 54HCT373**

**DG 10.1.2**

#### Rev B, 7/19/02